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(54) **MULTI-PROCESSOR MOBILE COMPUTER SYSTEM HAVING ONE PROCESSOR INTEGRATED WITH A CHIPSET**

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(58) **Field of Search** 700/4–5, 2, 82; 968/535; 713/320–324, 340

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,142,684	A *	8/1992	Perry et al.	713/320
5,239,495	A *	8/1993	Nanno et al.	713/321
5,410,713	A *	4/1995	White et al.	713/330
5,504,908	A *	4/1996	Ikeda	713/300
5,737,613	A *	4/1998	Mensch, Jr.	713/322
5,901,322	A *	5/1999	Herbst et al.	713/322
6,023,641	A *	2/2000	Thompson	607/9
6,029,249	A *	2/2000	Atkinson	713/323
6,311,287	B1 *	10/2001	Dischler et al.	713/601
2001/0003206	A1 *	6/2001	Pole et al.	713/320

FOREIGN PATENT DOCUMENTS

EP 0617812 B1 * 3/1998 ..... G06F/1/32

* cited by examiner

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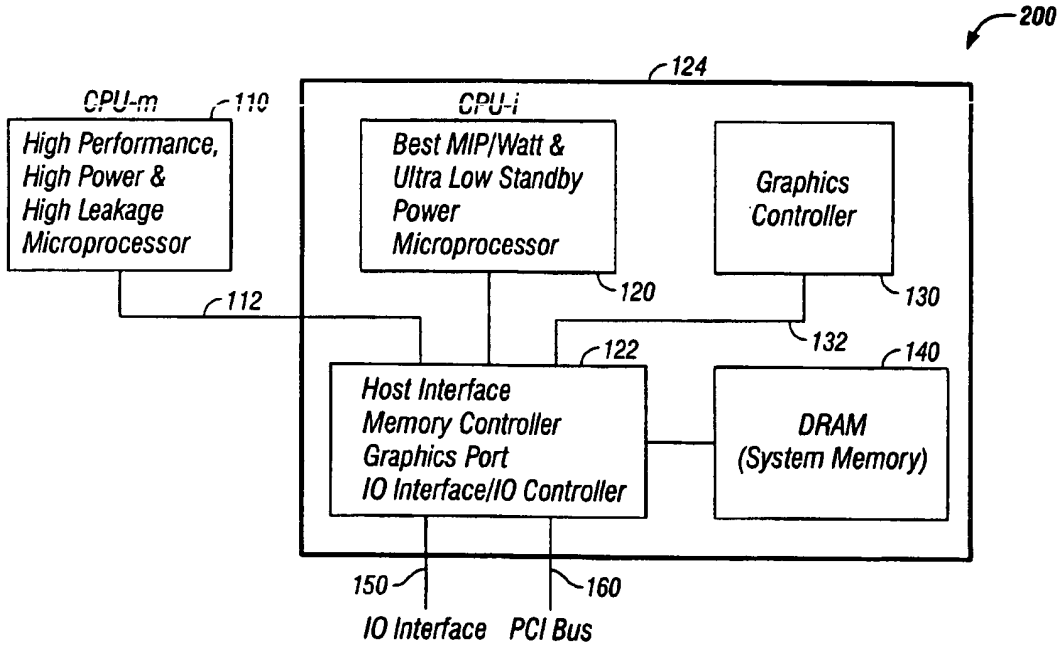
(57) **ABSTRACT**

Computer systems having two processors of different clock frequencies and different levels of power consumption. An interface circuit can select one of the two processors to operate at a time to reduce power consumption without compromising the system performance.

19 Claims, 3 Drawing Sheets



rupt RAM for keeping the CPU states during a transition may be integrated on the chip **124** with the power-efficient processor **120** to reduce the latency, although it may be a separate unit on the motherboard. The latency may be further reduced when the power-efficient processor **120** begins reading the CPU states at the same time while the high-performance processor **110** sends its CPU states to the chip **124**. A reverse process takes place when the execution is switched from the power-efficient processor **120** to the high performance processor **110**.

Another way to reduce the transition latency is to allow direct transfer between registers of the two processors through the bus **112** by using specific pin connections or a new instruction. In addition, a software routine, e.g., operating systems or the BIOS, for the processors **110** and **120** can be designed to maintain the configuration of the dormant processor to be the same as the active processor without transferring all CPU states between them. A further transition scheme uses the processor snooping during HALT/STOP GRANT mode of the dormant processor to allow transfer of CPU states of the active processor to the dormant processor when the power is off for all CPU logics except the minimum number of logics for snooping or for controlling the I/O interface bus.

The mobile computer system **100** of FIG. **1** can be highly integrated in part by fabricating the power-efficient processor **120** and other devices on the same chip **124**. This is possible because the power-efficient processor **120** is designed based on a mature processing technology that can be used to fabricate other integrated circuits of the system **100**. The supplying voltage Vcc for the power-efficient processor **120** can be relatively high and hence compatible with voltages of other circuits and devices while still maintaining the number of millions of instructions per watt at a desired high level for the power-efficient processor **120**. As a result, many devices and components of the system **100** may be integrated with the power-efficient processor **120** on the chip **124**.

For example, FIG. **2** shows a modified two-processor system **200** based on the system **100** in FIG. **1**. The graphic controller **130** and the system memory **140** are integrated with the processor **120** and the chipset **122** on the chip **124**. The power to the processor **120** and the power to the chipset **122** and other devices on the chip **124** may be separately controlled. Hence, when it becomes desirable to turn off the power to the processor **120** when the processor **110** is operating, the chipset **122** and other devices can still be powered to perform their functions.

The high-performance processor **110** may be separated from the chip **124** to allow necessary upgrade to faster high-performance processors. This design can considerably reduce the system cost because the life cycle of high-performance processors is generally longer than life cycles of chipsets **122**, the graphic controller, and other computer devices and components.

The above two-processor mobile computer systems are not limited to a power-saving mode in which only one of the two processors is operating at any given time while the other is dormant, and a high-performance mode in which the high-performance processor **110** is operating at all times while the power-efficient processor **120** is dormant. Such systems may be further configured to operate in a concurrent multiprocessing mode in which the two processors **110** and **120** can execute instructions of different program tasks or threads at the same time. A configuration register can be implemented, e.g., on the chip **124**, to determine which one of the three modes the system should operate at a request of the user or a command by an application or some control circuit in the system.

In one implementation of the concurrent multiprocessing mode, multiple programs or multithreaded programs can be run through each of the two processors **110** and **120**. In another implementation, the high-performance processor **110** may be designated as the main processor to run computation-intensive applications while the power-efficient processor **120** may be designated as the supplementary processor to run applications that do not demand high computation power. For example, the processor **120** may be an intelligent I/O processor to run local programs and to manage I/O devices.

Hence, the systems **100** and **200** may be configured to operate in either a serial mode in which the processors **110** and **120** in combination behave as a single processor, or in a concurrent mode in which both processors **110** and **120** can operate at the same time. FIG. **3** shows three different exemplary operating states based on the two modes for the systems **100** and **200**. Switching between the two modes can be done by resetting the configuration register based on the operating conditions and performance requirements for different applications. The operating system, the BIOS, or an application may be used to reset the configuration register.

The two processors **110** and **120** in general may be formed from any suitable processors. They may have different architectures or operate on different operating systems or different instruction sets. Sometimes the differences between the processors **110** and **120** can present problems. A proper interfacing mechanism can be used to harmonize the two processors **110** and **120** when necessary. The interfacing mechanism may be implemented in hardware, software, or a combination of both.

For example, instruction sets of the processors **110** and **120** may be different. Hence, an instruction for the high-performance processor **110**, that is required to carry out an operation of an application program running on the system, may not exist in the instruction set of the power-efficient processor **120**. Hence, in order to use the processor **120** to carry out the instruction, the interfacing mechanism may be designed to use a combination of native instructions for the power-efficient processor **120** to perform the instruction. When the combination does not exist, the processor **110** may need to be used, even when the power-saving operation demands operation by the power-efficient processor.

Although only a few embodiments are disclosed, other modifications and variations are contemplated.

What is claimed is:

1. A computer system, comprising:

a first processor, operating at a first clock frequency and a first level of power consumption;

a second processor of a second clock frequency and a second level of power consumption, said second clock frequency and second level being respectively less than said first clock frequency and said first level of power consumption; and

an interface circuit, coupled to control said first and second processors to select one processor to operate at a particular time, wherein electric power to said first-processor is turned off when said second processor is selected to operate.

2. A computer system as in claim **1**, further comprising a chipset that controls the communication among said first and second processors, wherein said interface circuit is built into said chipset, and wherein said second processor and said chipset are integrated on a single substrate.